## REMARKS/ARGUMENT

Claims 14-33 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite. The claims have been carefully amended to overcome these informalities. These changes do not narrow the scope of the claims.

With particular reference to claim 24, it is noted that Applicant has, where appropriate, named the various insulating films. However, to the extent that a separate name (e.g. first, second, third, insulating film) is not given, the claim is none the less definite. This is because in each case the location of the film or pad is clearly stated. If, for any reason, the Examiner continues to believe that there is an ambiguity in the claims, it is requested that he conduct a telephone interview with the undersigned in an effort to overcome such informalities.

Claims 14, 15, 19-26 and 28-33 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sato in view of Shiue, et al. The Examiner's rejection on this ground is respectfully traversed.

In accordance with the method of Applicant's invention, the semiconductor device includes a plurality of layers, at least two of which include a pad layer and an insulating film covering the pad layer. A plurality of through holes are formed in each of the insulting films and filled with a conductive material which extends from the pad layer to the top of the insulating film. As shown, by way of example, in Figure 1, each subsequent pad layer 20, 26 is in contact with the conductive material in the through holes in the immediately preceding insulating film. This corresponds generally to the structure shown

in Figure 12 of Sato. It also corresponds generally to the prior art described with reference to Figure 8 of Applicant's drawings.

Among the limitations of claim 23 which are neither disclosed nor suggested in Sato is the act of "(m) forming a bonding pad on the third conductor pad in the through hold in the third interlayer insulating film." Among the limitations of claim 24 which are neither disclosed nor suggestive in Sato is the act of "forming a bonding pad on the conductor pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film."

These features of Applicant's invention are clearly not shown in Sato. In his rejection, the Examiner has referred to Figure 23A of Sato as showing this feature of Applicant's claims. Particularly, the Examiner has asserted that Sato teaches the act of "forming a binding pad on the third conductor pad in the through hole". However, Figure 23A does not teach that such a process should be used in a multilayer structure such as that shown in Figure 11 of Sato and as set forth in Applicant's claims. Quite to the contrary, Sato teaches that the structure of Fig. 25A is not appropriate for a multilayer structure as in Applicant's invention. Particularly, Sato describes Figure 23A as prior art which teaches the desirability of utilizing a binding pad in the single layer structure of Figure 23A. However, he teaches that such a bonding pad is not desirable in a multi-layer structure such as that shown in Figures 3, 12 and 23C of Sato (Sato describes Fig. 23C as showing his invention). Sato teaches that a bonding pad is not required because the multilayer structure of Figure 23C itself will achieve a desired binding resistance:

> "The structure of FIG. 23C according to the present invention (i.e., the Structure 2 in Table 1) provides support columns 9500a, 9500b

> formed by conductors to *absorb the binding impact* , as show in FIG. 25. Thus, a crack less tends to be created in the interlayer insulating film (e.g., $CVD_1O_2$ film). According to the structure of the present invention, therefore, the bondability can be enhanced." [Emphasis added.]

See, 5 lines 60-66 of Sato.

Stated otherwise, Sato teaches that the bonding problems of the prior art can be overcome in the multi-layer structure of Figures 3, 12 and 23C without the use of the separate bonding pad of Figure 23A. In contrast, Applicant has recognized the need for such a bonding pad in the multi-layer structure of the present invention.

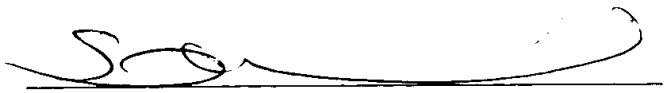
In view of the foregoing, it is strenuously submitted that Applicant's processes, as defined in claims 23 and 24 are neither disclosed nor suggestive in the art of record and that these claims are presently in condition for allowance.

The remaining claims all depend from claims 23 or 24 and recite all of the limitations found therein. These claims recite additional limitations which, in combination with limitation of claims 23 and 24, are neither disclosed nor suggested in the art of record. Accordingly, these claims are also in condition for allowance.

Applicant is pleased to note that the Examiner has indicated that claim 16-18 and 27 are directed toward patentable subject matter. Applicant has not rewritten these claims in independent form at this time since it is believed that the independent claims from which they depend are also in condition for allowance.

In view of the foregoing, it is believed that the application is now in condition for allowance. Reconsideration and allowance of the application is solicited.

Respectfully submitted,



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## APPENDIX A
## Version With Markings To Show Changes Made
## 37 C.F.R. § 1.121(b)(1)(iii) AND (c)(1)(ii)

CLAIMS:

14. (Amended) A method of manufacturing a semiconductor device according to claim 23, [according to claim 24,] further comprising:

[(d)] forming a passivation film on the third interlayer insulating film [of the upper layer], the passivation film exposing the bonding pad.

16. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step [(b)(2)] (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a [first] ceramic silicon oxide film; and

forming a [thick] second silicon oxide film on the [first] ceramic silicon oxide film by plasma CVD.

19. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step [(b)(4)] (e) comprises the steps of:

forming Ti [interlayer insulating] films covering [an] inner [surface] surfaces of the through holes in the first interlayer insulating film of the base layer;

forming TiN layers on the Ti [interlayer insulating] films; and

forming W layers on the TiN layers.

20. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step [(b)(4)] (e) comprises:

forming Ti [interlayer insulating] films covering [an] inner [surface] surfaces of the through holes in the first interlayer insulating film [of the base layer] by sputtering;

forming TiN layers on the Ti [interlayer insulating] films by sputtering; and

forming W layers on the TiN layer.

21. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step [(b)(4)] (e) comprises:

forming Ti [interlayer insulating] films covering [an] inner [surface] surfaces of the through holes in the first interlayer insulating film [of the base layer];

forming TiN layers on the Ti [interlayer insulating] films; and

forming W layers on the TiN [layer] layers by [blanket] plasma CVD.

22. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step [(b)(1)] (b) of forming the first conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

23. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a first conductive pad on the insulating film;

(c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) forming a second conductive pad on the first interlayer insulating film [and] in contact with the conductive material in the plurality of first through holes;

(g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

24. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;

(2) forming [an] a base layer insulating film on both the conductive pad and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film [of the base layer and extending] which through holes extend from the conductive pad to an upper surface of the base layer insulating film [of the base layer];

(4) filling the base though holes [formed in the insulating film of the base layer] with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following [acts] steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming [an] a respective interlayer insulating film on both the conductive pad [of the respective intermediate layer] and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes [and] extending from the conductive pad of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following [acts] steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film [of the upper layer], said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film [of the upper layer].

25. (Amended) A method of manufacturing a semiconductor device according to claim 24, [according to claim 24,] further comprising:

(e) forming a passivation film on the upper layer insulating film [of the upper layer], the passivation film exposing the bonding pad.

27. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a [first] ceramic silicon oxide film; and

forming a [thick] second silicon oxide film on the [first] ceramic silicon oxide film by plasma CVD.

28. (Amended) A method of manufacturing a semiconductor device according to claim [24] 27, further comprising a step of planarizing the second silicon oxide film by CMP.

29. (Amended) A method of manufacturing a semiconductor device according to claim [24] 27, further comprising a step of planarizing the second silicon oxide film by etching.

30. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti [interlayer insulating] films covering an inner surface of the through holes in the base layer insulating film [of the base layer];

forming TiN layers on the Ti [interlayer insulating] films; and

forming W layers on the TiN layers.

31. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti [interlayer insulating] films covering an inner surface of the through holes in the base layer insulating film [of the base layer] by sputtering;

forming TiN layers on the Ti [interlayer insulating] films by sputtering; and

forming W layers on the TiN layer.

32. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti [interlayer insulating] films covering an inner surface of the through holes in the base layer insulating film [of the base layer];

forming TiN layers on the Ti [interlayer insulating] films; and

forming W layers on the TiN layer by blanket CVD.

33. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step [(b)(1)] (c) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

## APPENDIX B

CLEAN VERSION WITHOUT AMENDED/NEW INDICATIONS

37 C.F.R. § 1.121 (c)(3)

**CLAIMS:**

14. (Amended) A method of manufacturing a semiconductor device according to claim 23, further comprising:

forming a passivation film on the third interlayer insulating film, the passivation film exposing the bonding pad.

16. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

19. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (e) comprises the steps of:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film of the base layer;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers.

20. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (e) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layer.

21. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (e) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers by plasma CVD.

22. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (b) of forming the first conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

23. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a first conductive pad on the insulating film;

(c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) forming a second conductive pad on the first interlayer insulating film [and] in contact with the conductive material in the plurality of first through holes;

(g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

24. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;

(2) forming a base layer insulating film on both the conductive pad and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film which through holes extend from the conductive pad to an upper surface of the base layer insulating film;

(4) filling the base though holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on both the conductive pad and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes extending from the conductive pad of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

25. (Amended) A method of manufacturing a semiconductor device according to claim 24, further comprising:

(e) forming a passivation film on the upper layer insulating film, the passivation film exposing the bonding pad.

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27. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

28. (Amended) A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by CMP.

29. (Amended) A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by etching.

30. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers.

31. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layer.

32. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layer by blanket CVD.

33. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (c) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.